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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,557	01/12/2001	John Lee Barry	04148P013	9690

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EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	6

DATE MAILED: 07/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/759,557	BARRY ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) *31-48 and 50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 49* is/are rejected.

7)☒ Claim(s) *10 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5* .
4) ☒ Interview Summary (PTO-413) Paper No(s). *6* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-30 and 49, drawn to Pattern Generation, classified in class 714, subclass 738.

   II. Claims 31-48 and 50, drawn to BIST circuitry, classified in class 714, subclass 733.

The inventions are distinct, each from the other because of the following reasons: Inventions Group I, Pattern Generation, and Group II, BIST circuitry, are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I, Pattern Generation, has separate utility such as in external testing. See MPEP § 806.05(d).

Inventions Group II, BIST circuitry, and Group I, Pattern Generation, are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group II, BIST circuitry, has separate utility such as for testing where a stored signature is used. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Andre Marais on 22 July 2003 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-30 and 49. Affirmation of this election must be made by applicant in replying to this Office action. Claims 31-48 and 50 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in

the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Oath/Declaration

The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

2. The oath or declaration is defective because:

The Declaration does not include a signature for each applicant.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: "56" in Figure 1C and 4B, and "342" in Figure 10. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claims

4. The Examiner notified the Attorney, Andre Marais, on 22 July 2003 that the claims had been renumbered to remove duplicate numbering of claims. No further action is required by the Attorney.

Claim Objections

5. Claims 10 and 25 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The Examiner asserts that functional verification of a circuit is a built-in self-test step, that is, the built-in self-test is being performed whenever the circuit is being verified, hence claims 10 and 25 as stated provide no additional limitations to claims 1 and 16.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 22-24 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22 recites the limitation "The test circuit" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claims 23 and 24 depend from claim 22, hence inherit the deficiencies of claim 22.

Claim 30 cites similar language as in claim 22.

The Examiner is assuming that the Applicant intended claim 22 to depend from claim 16 and claim 30 to depend from claim 29.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-30 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jarwala, Najmi T. et al. (US 5444716 A, hereafter referred to as Jarwala).

35 U.S.C. 103(a) rejection of claims 1 and 16.

Jarwala teaches a method and a test circuit of generating test data to functionally verify a circuit (TVO memory 32 for storing deterministic test vectors, Automatic Test Pattern Generator ATPG 34 and MUX 36 in Figure 2 of Jarwala is a test circuit providing a method for generating test data to functionally verify a circuit), the method comprising: detecting a data selection signal; responsive to the data selection signal, presenting test data to verify the circuit, wherein the presenting of the test data includes composing the

test data utilizing a combination of Automatic Test Pattern Generator (ATPG) generated data and stored data (Note: MUX 36 in Figure 2 of Jarwala is a device for detecting a data selection signal used to control input selection and, responsive to the data selection signal used to control input selection, presenting test data to verify the circuit, wherein the presenting of the test data includes composing the test data utilizing a combination of ATPG generated data and stored data).

However Jarwala, does not explicitly teach the specific use of algorithmically generated data.

The Examiner asserts that it would be obvious based on engineering design choices to replace the ATPG in Jarwala with an Algorithmic Pattern Generator (ALPG). One of ordinary skill in the art at the time the invention was made would have been highly motivated to replace the ATPG in Jarwala with an ALPG since one of ordinary skill in the art at the time the invention was made would have know that an ALPG significantly reduces test pattern data volume and increases test efficiency.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Jarwala by including use of algorithmically generated data. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of algorithmically generated data would have provided the opportunity to significantly reduce test pattern data volume and increase test efficiency.

35 U.S.C. 103(a) rejection of claims 2 and 17.

State machine generated data is algorithmically generated data; hence see rejection to claims 1 and 16, above.

35 U.S.C. 103(a) rejection of claims 3 and 18.

In col. 5, lines 50-58, Jarwala teaches that the test circuit is IEEE 1149.1 compliant; the IEEE 1149.1 Test Access Port (TAP) is a state machine.

35 U.S.C. 103(a) rejection of claims 4 and 19.

The output of MUX 36 in Figure 2 of Jarwala is a data stream.

35 U.S.C. 103(a) rejection of claims 5 and 20.

A video test pattern is still a test pattern for testing a circuit (see rejections to claims 1, 4 16 and 19, above).

35 U.S.C. 103(a) rejection of claims 6 and 21.

A packet comprising test data is still digital test data (see rejections to claims 1, 4 16 and 19, above). In addition, see Figure 3 in Jarwala.

35 U.S.C. 103(a) rejection of claims 7 and 22.

The Abstract in Jarwala teaches test data is supplied to circuit boards to test the functionality of the circuit boards. Circuit boards are a system or part of a system.

35 U.S.C. 103(a) rejection of claims 8, 9, 23 and 24.

Video test data is still digital test data (see rejections to claims 1, 4 16 and 19, above). In addition, col. 7, lines 44-51 teach BIST circuitry for testing.

35 U.S.C. 103(a) rejection of claims 10 and 25.

The Examiner asserts that functional verification of a circuit is a built-in self-test step hence the built-in self-test is being performed whenever the circuit is being verified.

35 U.S.C. 103(a) rejection of claims 11,12, 26 and 27.

Col. 7, lines 5-40 in Jarwala teach the use of checksum generators whereby verification is performed by checking if the checksum values match.

35 U.S.C. 103(a) rejection of claims 13 and 28.

CRC is a block code, hence; the CRC checksum is performed for each block within the data stream, each block being a specific point within the data stream.

35 U.S.C. 103(a) rejection of claims 14 and 29.

The Abstract in Jarwala teaches that test information is sent to the host; note: test data is test information.

35 U.S.C. 103(a) rejection of claims 15 and 30.

A digital television system is still a digital system (see rejections to claims 1, 4 16 and 19, above).

35 U.S.C. 103(a) rejection of claim 49.

Jarwala provides block diagrams of the test circuitry, which are a design for manufacture (see Figures in Jarwala and rejections to claims 1, 4 16 and 19, above).

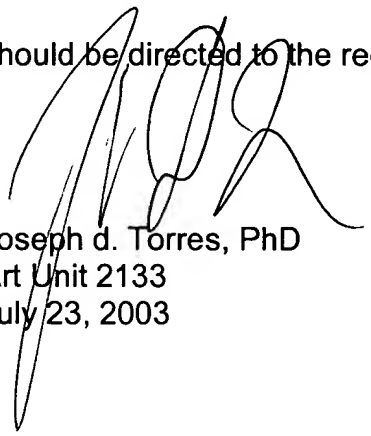
Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rajski, Janusz et al. (US 5991909 A) teaches a parallel decompressor capable of concurrently generating in parallel multiple portions of a deterministic partially specified data vector is disclosed. Maeno, Hideshi et al. (US 4813043 A) teaches an ALU unit with shift-in function for conducting a predetermined arithmetical and logical operation against the base data or the output of an ALU output register; the ALU output register being designed to store the output of the ALU and output a function test algorithmic pattern. Keller, Paul N. et al. (US 5479414 A) teaches a look-ahead pattern generation and simulation scheme for algorithmically generated test patterns to reduce test pattern data volume and increase test efficiency.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.



Joseph d. Torres, PhD
Art Unit 2133
July 23, 2003